VLSI DESIGN OF DISCRETE WAVELET PACKET TRANSFORM FOR WIRELESS LOCAL AREA NETWORKS

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Abstract:

The global market for wireless local area networks (WLANs) is expected to reach approximately $60 billion by 2025, driven by the increasing demand for high-speed internet connectivity and data- intensive applications. As WLAN technology evolves, the need for efficient signal processing methods becomes paramount, with the DWT commonly used for data compression and noise reduction. However, existing DWT implementations face significant challenges, including high computational complexity and limited scalability, which can hinder performance in real-time applications. This paper proposes a DWPT method specifically designed for VLSI implementation in WLANs. By enhancing the traditional DWT framework, the proposed DWPT method optimizes the signal processing chain, achieving better frequency resolution and improved energy compaction. This novel approach integrates a pipelined architecture that significantly reduces processing time and power consumption, making it ideal for resource-constrained environments such as mobile and embedded systems. The implementation of the DWPT not only addresses the limitations of existing DWT methods but also enhances the overall performance of WLAN systems. The advantages of the proposed method include improved compression efficiency, reduced computational complexity, enhanced real-time processing capabilities, lower power consumption, and scalability for future wireless applications.

Keywords: Wireless Local Area Networks (WLANs), Signal Processing, Computational Complexity, Discrete Wavelet Transform (DWT), Discrete Wavelet Packet Transform (DWPT)

1. INTRODUCTION

Wavelet transformation in communication involves analysing signals with wavelets to capture both frequency and time-domain information. It offers advantages like localized signal analysis and efficient data compression. In communication, wavelets are used for tasks such as signal demonising, modulation recognition and efficient coding, enhancing the understanding and transmission of information. The ability to represent signals at different scales makes wavelet transformation valuable in diverse communication applications, including image and audio processing. Wavelet transformations play a significant role in communication systems, offering advantages in signal processing, compression, and analysis.

Wavelets provide a multi-resolution analysis, allowing the decomposition of a signal into different frequency components at various resolutions. This is particularly useful in communication systems where signals often have diverse frequency components. Wavelet transformations were applied to compress signals efficiently. By representing a signal in the wavelet domain, it becomes possible to focus on the most relevant information, reducing redundancy and achieving better compression ratios. This is crucial in communication for efficient data transmission and storage.

Unlike traditional Fourier transformations, wavelet transformations offer an adaptive representation of signals. This adaptability is valuable in communication scenarios where the characteristics of the signal change over time or under varying conditions. Wavelets have excellent time and frequency localization properties. This is advantageous in communication systems for analysing signals in both the time and frequency domains simultaneously, allowing for precise identification of events and features.

Wavelet transformations were employed for demonising signals. In communication, this is crucial to enhance the quality of received signals by removing unwanted noise or interference. Wavelet transformations was used in modulation and demodulation processes. They provide a flexible framework for analysing and manipulating signals during the modulation/demodulation stages, contributing to improved efficiency and reliability in communication.

2. LITERATURE SURVEY

Pritiranjan, et al. [1] implemented the complex harmonic wavelet (CHW) was being used to directly compute frequency content with respect to time by employing discrete Fourier transform (DFT) and inverse DFT (IDFT). However, DFT coefficients suffer severe leakage of energy from one band to another band of frequency. The leakage between bands was minimized by employing discrete cosine transform (DCT) in the harmonic wavelet transform (HWT), which leads to a better representation of the time–frequency spectrum. This article introduces a new VLSI architecture for DCT -based harmonic wavelet for hardware implementation and prototyped on a commercially available virtex5 field-programmable gate array (FPGA) (xc5vlx110t). To validate the proposed implementation, its real-time captured results in the logic analyzer were verified with simulation results. The maximum operating frequency targeting the FPGA mentioned above device was reported as 114.34 MHz The total ON-chip power of the above implementation was 1.102 W, out of which 68 mW is the dynamic power dissipation at a toggle

rate of 12%. Finally, for the area utilization of the above implementation.Its resource utilization targeting the above FPGA device was reported.

They examined the effects of quantization on DWT performance in classification problems to demonstrate its reliability concerning fixed-point math implementations. The Advanced Encryption Standard (AES) algorithm for DWT learning used in this architecture was less responsive to re-sampling errors than the previously proposed solution in the literature using the artificial neural networks (ANN) method. By reducing hardware area by 57%, the proposed

system had a higher throughput rate of 88.72%, reliability analysis of 95.5% compared to the other standard methods.

Pranose J.Edavoor, et al. [2] was proposed this article presents a novel generalized approach to obtain rational (dyadic and integer) bi- orthogonal wavelet filter coefficients based on two conditions, namely maximally flatness and near-perfect reconstruction (PR) in half-band polynomial (HBP). An incremental-iterative approach was adopted to design the coefficients based on the proposed error equation in terms of the remainder polynomial (RP) of Lagrange HBP and the proposed HBP with maximum vanishing moments (VMs). In addition, VLSI architecture for the proposed wavelet filter banks (FBs) was designed and implemented on the Zedboard ZYNQ- 7000 AP-SoC (Zynq FPGA from Xilinx) field-programmable gate array. It was found that the proposed rationalized wavelet FBs achieved significantly low digital hardware requirements with similar characteristics when compared to well-known rationalized existing bi-orthogonal wavelet FBs. The effectiveness of the designed wavelet FBs was verified in image compression and image retrieval on well- known publicly available databases. It was found that the designed rationalized bi-orthogonal wavelet FBs give better performances when compared to existing rationalized bi-orthogonal wavelet FBs.

Morgana MA Rosa, et al. [3] this work discovered an ultra-low- energy ECG data compression with VLSI DHWT-based (discrete Haar wavelet transform) architecture to enable storage and transmission in resource-constrained environments. We present original, pruned, and approximate DHWT (ODHWT, PDHWT, and AxDHWT, respectively) hardware architectures for ECG data compression at ultra-high energy efficiency. Our best proposal employing the AxDHWT hardware architecture requires just five additions only. Using a PDHWT technique to improve energy efficiency observes the evolution of the signal-to-noise ratio and the ultimate impact on the ECG data compression application. The DHWT-based configurations architecture proposal achieved a minimum compression ratio of 0.125 (i.e., 1/8) and a PRD (percent root difference) <1.34. The AxDHWT occupies a die area of 0.64mm ^{2}. The measured total power is 0.534μW, the higher energy- savings among the ECG data compression architectures.

Marimuthu Mohanapriya, et al. [4] introduced continuous improvements in very-large-scale integration (VLSI) technology and design software have significantly broadened the scope of digital signal processing (DSP) applications. The use of application-specific integrated circuits (ASICs) and programmable digital signal processors for many DSP applications have changed, even though new system implementations based on reconfigurable computing are becoming more complex. New research and commercial efforts to sustain power optimization, cost savings, and improved runtime effectiveness had been initiated as initial reconfigurable technologies have emerged. Hence, in this literature, it is proposed that the DWT method was implemented on a field-programmable gate array in a digital architecture (FPGA-DA). We examined the effects of quantization on DWT performance in classification problems to demonstrate its reliability concerning fixed-point math implementations. The Advanced Encryption Standard (AES) algorithm for DWT learning used in this architecture was less responsive to re-sampling errors than the previously proposed solution in the literature using the artificial neural networks (ANN) method. By reducing hardware area by 57%, the proposed system had a higher throughput rate of 88.72%, reliability analysis of 95.5% compared to the other standard methods.

K.R. Venugopal, et al. [5] discovered the detection of Salient objects in image and video sequences were very interesting and rewarding task which was the crux of many applications that deal with computer vision. Salient objects were segmented from the objects of interest and were correlated with objects in its neighborhood which was similar to the cognitive property of human visual system. Major distinction of using complex wavelets in the process of salient object

detection lies in the fact that the complex wavelets had the directional selectivity property. Systolic Array and Distributive architectures are considered for the detection of salient objects in the video sequence using 3D DTCWT. The proposed work were implemented on SPARTAN 6 FPGA and tested in the XILINX.

Mannepalli Vishnu, et al. [6] implemented many conventional signal processing methods have been applied in the image fusion field to extract image features, such as DWT, contourlet transform, shift-invariant shearlet transform and quaternion wavelet transform etc. For the infrared and visible image fusion task. But these methods introduce artifacts into the fused image. To overcome these problems optimization based fusion schemes were proposed. These methods take multiple iterations to find the optimal solution (fused image). These optimization methods over smooth the fused image because of multiple iterations. This work focused on hardware-oriented implementation of VLSI based implementation of VI-IR image fusion mechanism. Initially, images are read using Matlab environment. Then, stationary wavelet transform was applied to decompose the VI, and IR images into multiple bands. The low-low bands were converted into text files. Further, the band fusion rule was applied on low-low bands, where multiplexer-based adder was used to combine both images. Finally, Matlab environment was used to reconstruct the fused image from the obtained text files. The simulation results show that the proposed method resulted in better performance.

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3. PROPOSED METHODOLOGY

Wavelets are mathematical functions that decompose data into different frequency components and analyse them at various scales. Unlike traditional Fourier analysis, which decomposes signals into sinusoidal functions of different frequencies, wavelet analysis employs functions that are localized in both time and frequency. This localization property allows wavelets to capture both short-duration and long-duration features of a signal with high precision. By convolving the signal with a wavelet function at different scales and positions, wavelet analysis generates a detailed representation of the signal's time-frequency content, revealing important information such as transient events, abrupt changes, and frequency variations. In practical applications, wavelets find extensive use in signal processing tasks such as demonising, compression, feature extraction, and time-frequency analysis. They offer advantages over traditional Fourier methods by providing better time resolution for transient signals and improved frequency resolution for signals with non- stationary behaviour. Additionally, wavelet transforms can adaptively adjust their analysis window size to capture signal features at different scales, making them particularly suitable for analysing complex signals encountered in fields such as image processing, biomedical engineering, audio processing, and financial data analysis.

3.1 Block Diagram of DWPT

To comprehend the basic operation of a Discrete Wavelet Packet Tree (DWPT) for a 3-level 8-point signal, we must first understand the fundamentals of wavelet packet decomposition and its application in signal processing tasks. Wavelet packet decomposition extends the concept of wavelet transform by allowing for a more comprehensive analysis of signals at various resolutions and frequency bands.

In a 3-level 8-point DWPT, the signal undergoes three stages of decomposition, resulting in a tree structure with multiple nodes representing different frequency components.

At the outset, the signal is represented as a vector of 8 data points. In the first stage of decomposition, the signal is split into two subspaces using a low-pass filter (LPF) and a high-pass filter (HPF). The LPF captures the low-frequency components of the signal, while the HPF captures the high-frequency components. These results in two sub-spaces often referred to as approximation (A) and detail (D) coefficients. The approximation coefficients represent the coarsest level of approximation of the signal, while the detail coefficients capture finer details and high-frequency components.

At the second stage of decomposition, each subspace resulting from the first stage undergoes a similar splitting process. The approximation coefficients from the first stage are split again using LPF and HPF filters, resulting in four subspaces: AA, AD, DA, and DD. Similarly, the detail coefficients from the first stage are split to produce four additional subspaces: VV, VH HV, and HH. These subspaces represent different combinations of low-pass and high-passfiltered components, capturing both horizontal and vertical details of the signal.
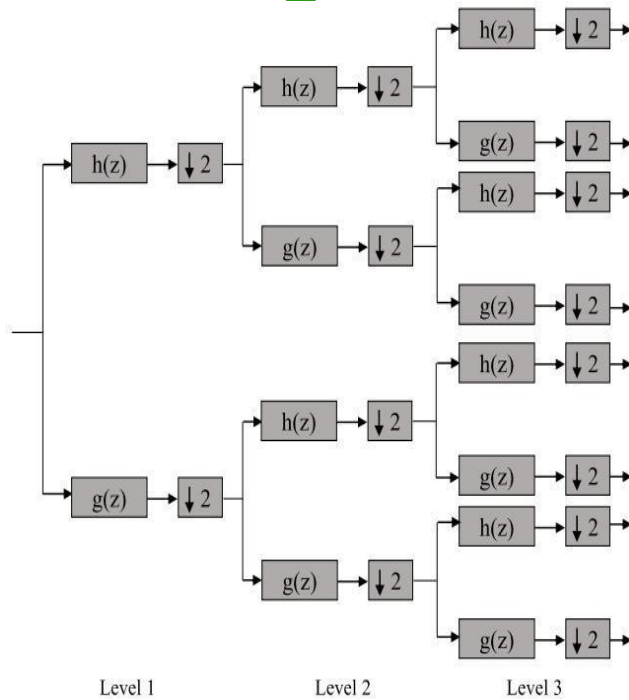
Figure 3.1: Block Diagram of DWPT

In the third and final stage of decomposition, each subspace resulting from the second stage undergoes another round of splitting using LPF and HPF filters. This yields a total of eight subspaces: AAA, AAD, ADA, ADD, DAA, DAD, DDA, and DDD. These subspaces represent increasingly finer details and frequency components of the original signal, allowing for a comprehensive analysis of the signal's spectral characteristics.

The resulting tree structure from the 3-level 8-point DWPT represents a hierarchical organization of the signal's frequency components. At the root of the tree lies the original signal, which branches out into multiple nodes representing different frequency bands and resolutions. The nodes at the lowest level of the tree contain the most detailed information about the signal, while the nodes at higher levels represent coarser approximations.

The operation of a full wavelet packet tree involves recursively decomposing the signal into its frequency components until a desired level of detail is achieved. Each decomposition stage involves splitting the signal into approximation and detail coefficients using LPF and HPF filters, resulting in a tree structure with multiple nodes representing different frequency bands and resolutions.

3.2 Overall DWPT Architecture

The operation described outlines a comprehensive process within a bypassed wavelet filter, a sophisticated signal processing technique used for various applications such as noise reduction, feature extraction, and data compression. Figure 4.4 shows the overall DWPT architecture. The detailed operation given as follows:

Step 1: Consider Input Data: At the onset of the filtering process lies the consideration of input data. This data serves as the raw material for the filtering operation, encapsulating the information that needs to be processed and refined. It originates from diverse sources such as sensor readings, audio recordings, or any other form of digital signal. Understanding the characteristics and nuances of the input data is crucial as it forms the foundation for subsequent processing steps.

Step 2: Generate Level Output: Following the consideration of input data, the next step involves generating the level output through a bypassed wavelet filter. This process entails applying wavelet decomposition to the input signal to extract different frequency components at various levels. Each level output represents a different scale or resolution of the original signal, thereby capturing both low- frequency and high-frequency details. This multi-level decomposition enables the filter to analyse the input signal across different frequency bands, providing insights into its spectral characteristics.

Perform Down-sampling Amplifier by Factor 2: Once the level output is generated, the filtering process proceeds to down-sample the output by a factor of 2. Down-sampling involves reducing the sampling rate of the signal, effectively decreasing the number of data points while preserving essential signal information. This down- sampling by a factor of 2 typically occurs in wavelet decomposition to accommodate the multi-resolution analysis of the input signal. By down-sampling, the filter optimizes computational efficiency while retaining key features of the signal, facilitating subsequent processingsteps.

Mux 2-to-1 Operation: Following down-sampling, the filtered data undergoes a multiplexing (mux) operation, which consolidates two input signals into a single output based on a control signal. In this operation, if the control signal is 0, indicating feedback, the output reflects the feedback signal. Conversely, if the control signal is 1, indicating feed-forward, the output represents the feed-forward weight. This mux operation provides flexibility in routing the filtered data, enabling the filter to adapt its processing strategy based on the prevailing conditions and requirements.

Mux Output Stored into Register: After the mux operation, the resulting output is stored into a register for temporary storage. This register

serves as a repository for holding the filtered data temporarily, facilitating subsequent processing steps. By storing the output into a register, the filter ensures that the data remains accessible for further analysis and manipulation as the filtering process progresses. This temporary storage mechanism allows the filter to maintain a record of the filtered data at different stages, enabling comparative analysis and validation.

Mux 2-to-1 Output Level 1 Output: In this final step, the output from the mux operation, which represents the filtered data, is directed to level 1 output. This output encapsulates the filtered signal at the first level of wavelet decomposition, reflecting the low-frequency components extracted from the input signal.

By directing the filtered data to level 1 output, the filter provides a glimpse into the foundational features of the input signal, facilitating further analysis and interpretation.
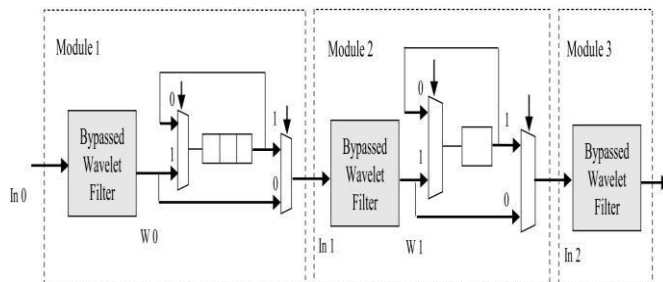
4. EXPERIMENTAL ANALYSIS

Figure 4.1 shows the existing simulation outcome.

Figure 4.2 shows the existing area measurements for N=8. Here 75 number of look up table (LUTS) are used out of available 133800, which consumes 0.06% of utilization, 40 number of FF are used out of 267600, which consumes 0.01% of utilization, 26 number of IO are used out of 500, which consumes 5.20% of utilization, 1 number of BUFG are used out of 32, which consumes 3.13 of utilization.

Step 3: Repeat the Operation for Multiple Levels and Generate the Outcome: The filtering process described above is repeated iteratively for multiple levels of wavelet decomposition. At each level, the input signal undergoes wavelet decomposition, down- sampling, multiplexing, and temporary storage, culminating in the generation of level output for that particular level. By repeating the operation for multiple levels, the filter dissects the input signal across different frequency bands, capturing both low-frequency and high-frequency details. The outcome of this iterative process is a multi- level representation of the input signal, providing insights into its spectral characteristics and temporal dynamics.
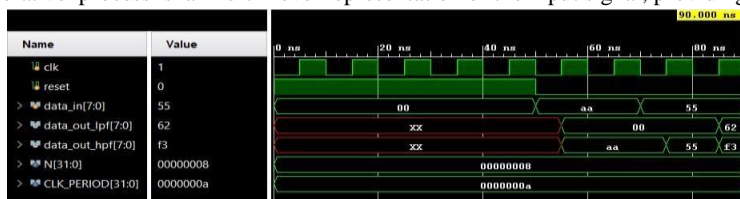

Figure 4.1. Existing Simulation Result for N=8

Advantages:

Improved Compression Efficiency: The proposed DWPT method enhances data compression, allowing for more efficient use of bandwidth in wireless networks.

Reduced Computational Complexity: The pipelined architecture minimizes processing delays, enabling faster signal processing and real-time performance.

Enhanced Real-Time Processing: The DWPT allows for quick transformations, making it suitable for high-speed applications in WLANs and other wireless technologies.

Lower Power Consumption: The optimization of the signal processing chain reduces power requirements, making the system more energy-efficient.

Scalability for Future Applications: The DWPT method is adaptable to evolving wireless standards, ensuring long-term viability in a rapidly changing technological landscape.

Applications:

Video Streaming: The DWPT can efficiently compress and transmit high-definition video content, improving user experiences in streaming applications.

Voice over IP (VoIP): Enhanced signal processing capabilities make DWPT ideal for delivering clear and reliable voice communications over wireless networks.

Online Gaming: The low latency and real-time processing of the DWPT support smooth game-play experiences in online multiplayer environments.

Wireless Sensor Networks: The efficiency of the DWPT allows for effective data transmission in sensor networks, enabling timely responses to environmental changes.

Telemedicine: The DWPT can facilitate secure and efficient transmission of medical images and data, enhancing remote healthcare services.

Resource	Utilization	Available	Utilization %
LUT	75	133800	0.06
FF	40	267600	0.01
IO	26	500	5.20
BUFG	1	32	3.13

Figure 4.2. Existing Area for N=8

Figure 4.3 shows the existing power measurements for N=8. Here dynamic power is 13.838W, the signals is 0.603W, the logic is 0.555W and the input/output is 12.680W.Here the static power is 0.153W, in PL static is 0.153W. Figure 6.4 shows the existing set up delay measurements for N=8. Here the set up delay consists of total 3delays they are, total delay is 7.459, logic delay is 3.980, and net delay is 3.479.
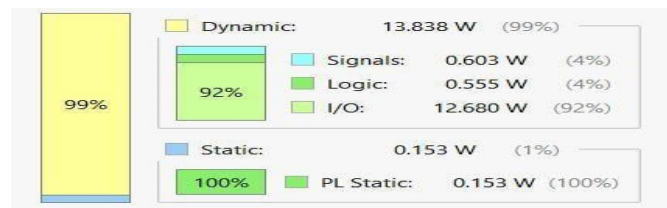

Figure 4.3. Existing Power for N=8

Figure 4.4 shows the proposed simulation outcome. Figure 6.7 shows the proposed area measurements for N=8. Here 9 number of look up table (LUTS) are used out of available 133800, which consumes 0.01% of utilization, 32 number of FF are used out of 267600, which consumes 0.01% of utilization, 26 number of IO are used out of 500, which consumes 5.20 of utilization, 1 number of BUFG are used out of 32, which consumes 3.13% of utilization.
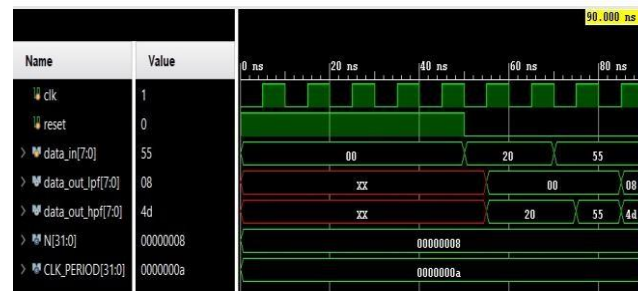

Figure 4.4. Proposed Simulation Result for N=8

Resource	Utilization	Available	Utilization %
LUT	9	133800	0.01
FF	32	267600	0.01
IO	26	500	5.20
BUFG	1	32	3.13

Figure 4.5. Proposed Area for N=8

Figure 4.6 shows the existing power measurements for N=8. Here dynamic power is 6.443W, the signals are 0.133W, the logic is 0.038W and the input/output is 6.271W. Here the static power is 0.131W. Figure 6.9 shows the proposed set up delay measurements for N=8. Here the set up delay consists of total 3 delays they are, totaldelay is 5.755, logic delay is 3.576, and net delay is 2.229. Figure
6.10 shows the proposed hold delay measurements for N=8. Here the set up delay consists of total 3 delays they are, total delay is 0.450, logic delay is 0.193, and net delay is 0.257.
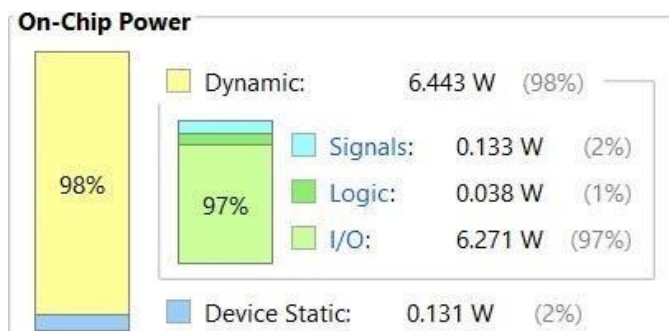

Figure 6.8: The Proposed power measurements for N=8.

5. CONCLUSION

In conclusion, the integration of DWPT into WLAN applications through VLSI technology offers a host of advantages that significantly enhance the efficiency, reliability, and performance of wireless communication systems. By focusing on optimizing hardware resources, minimizing power consumption, and meeting stringent performance requirements such as throughput and latency, VLSI-based DWPT implementations pave the way for seamless integration directly into WLAN transceivers. This not only simplifies system architecture but also reduces costs and form factors, making them particularly well-suited for integration into portable devices likeSmartphone's and tablets.

Moreover, DWPT with VLSI provides numerous benefits for WLAN systems, including efficient bandwidth utilization, enhanced signal integrity, and real-time processing capabilities, all while maintaining compatibility with existing standards like IEEE 802.11. By selectively transmitting relevant frequency components and mitigating the effects of channel impairments and interference, DWPT significantly improves the reliability and robustness of wireless communication. With the ability to facilitate faster data transmission and overall system performance enhancements, VLSI- based DWPT implementations are poised to play a pivotal role in the continued evolution of wireless technologies across a broad spectrum of WLAN applications.

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