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INTERINTED CIRCUIT DESIGN BASED ON VERILOG

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ABSTRACT

Inter-integrated circuit (I2C) design using Verilog in Modelsim Altera 6.4a (Quartus 2nd edition 9.0) is the main focus of this work.A straightforward and effective way to send data over a short distance between numerous devices is the I2C Bus, a two-wire, bi-directional serial bus. It has very low hardware resource requirements and offers good support for communication with a variety of sluggish, on-board peripheral devices that are used occasionally. It is a straightforward, short-range, low-bandwidth protocol that supports several masters. Data bytes can be sent and received by slaves and masters. The following are I2C's operational speed modes:

Standard-mode (Sm) – up to 100 kbps

Fast-mode (Fm) – up to 400 kbps

Fast-mode Plus (Fm+) – up to 1 Mbps

High-speed mode (Hs) – up to 3.4 Mbps.

KEYWORDS: Design firms like as Texas Instrument, Analog Devices, Intel, and others create I2C buses, Master, Slave, Finite State Machines, and Verilog ModelSim.

Introduction:

A straightforward and effective way to send data over a short distance between several devices is the I2C Bus, a two-wire, bi-directional serial bus. Chip-to-chip communications before I2C relied on a parallel interface with several pins. Numerous pins were utilized for data transfers, control, selection, and inter-chip addressing. Eight data bits are normally sent in a single operation from a transmitter IC to a receiver IC in a parallel link.ICs may connect with fewer pins thanks to I2C, which uses only two wires in a serial interface to conduct chip-to-chip communications. One bit at a time, the two wires that make up the I2C Bus transport data, control, selection, and addressing. While the Clock (SCL) wire keeps the sender and recipient in sync during the transmission, the Data (SDA) wire transports the data. With far fewer pins, integrated circuits (ICs) that utilize the I2C Bus may do the same task as their bigger parallel interface equivalents.I2C provides good support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardwareresource needs. It is a simple, low-bandwidth, short distance protocol. I2C is easy to use to link multiple devicestogether since it has a built-in address

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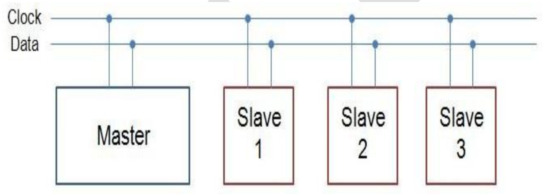
.The two I2C signals are serial data (SDA) and serial Clock (SCL).The device that initiates a transaction on the I2C bus is termed the master. The masternormally controls the clock signal. A device being addressed by the master is called a slave.

The I2C protocol supports multiple masters, but most system designs include only one. There may be one or more slaves on the bus. Both mastersand slaves can receive and transmit databytes. Standard I2C devices operate up to 100Kbps, while fast-mode devices operate at up to 400Kbps. Most of the I2C devices available today support 400Kbps operation. Higher speed operation may allow I2C to keep up withthe rising demand for bandwidth in multimedia and other applications.

In the figure below, there is one Master; the other devices are all Slaves. When a Master wants to initiate a communication, it issues a “START” condition. At that time, all devices, including the other Masters, have to listen to the bus for incoming data. Afterthe “START” is issued, the Master sends the “ADDRESS” of the Slave that it wishes to communicate with along with a bit to indicate the direction of the data transfer (either read or write). All Slaveswill then compare their addresses with the address received on the bus. If the addresses are identical, the Slave with the matching address will send an (ACK) “ACKNOWLEDGEMENT” to the Master.Slaves whose addresses do not match will not send an ACK. Once communication is established, the twolines are busy. No other device is allowed to control the lines except the Master and the Slave which was selected. When the Master wants to terminate communication, it will issue a “STOP” signal. After that, both SCL line and SDA line are released and free.



Block diagram of an i2c configuration.
Multiple integrated circuits are aligned on a two-wire bus. Assigning unique addresses allows a master device to control multiple slave devices.

1. MASTER AND SLAVE

The device that starts a data transfer on the bus and creates the clock signals necessary to allow it is known as a master. Any device that is addressed at that point is regarded as a slave. When the bus is not in use, both are linked to a positive supply by a pull-up resistor and stay HIGH.

Every device, whether it a microprocessor, LCD driver, memory, or keyboard interface, is identified by its own address and may function as a transmitter or receiver.
depending on the function of the device. A device generating a message or data is a transmitter, and a device receiving the message or data is areceiver.

A passive function like an LCD driver could only be a receiver, while a Micro controller or a memory can bothtransmit and receive data. When a data transfer takes place on the bus, a device can either be a master or a slave. The device which initiates the transfer, and generates the clock signals for this transfer, is the master. At that time any device addressed is considered a slave. It is important to note that a master could either be a transmitter or a receiver; a master microcontroller may send data to a RAM acting as a transmitter, and then interrogate the RAM for its contents acting as a receiver in both cases performing as the master initiating the transfer. In the same manner, a slave could be both a receiver and a transmitter. The I2C is a multimaster bus. It is possible to have, in one system, more than one device capable ofinitiating transfers and controlling thebus. A microcontroller may act as a master for one transfer, and then be the slave for another transfer, initiated byanother processor on the network. The master/slave relationships on the bus are not permanent, and may change on each transfer. As more than one master may be connected to the bus, it is possible that two devices will try to initiate a transfer at the same time. Obviously, in order to eliminate bus collisions andcommunications chaos, an arbitration procedure is necessary. The I2C design has an inherent arbitration and clock synchronization procedure relying on the wired-AND connection of the devices on the bus. In a typical multi master system, a microcontroller program should allow it to gracefully switch between master and slave modesand preserve data integrity upon loss of arbitration.

1.1 START AND STOP

When a Master wants to initiate a data transfer, it issues a Start condition and when it wants to terminate the transfer, a Stop condition will be initiated. Therecan be multiple Starts during one transaction called a repeated Start. The Master can then release the Stop condition whenever it wants to. In Figure, a Start is issued by bringing the SDA line low while the SCL line is high. After that the Master controls the SCL line and can generate clock signals. A Stop condition is implemented by transitioning the SDA line high while theSCL line is high.

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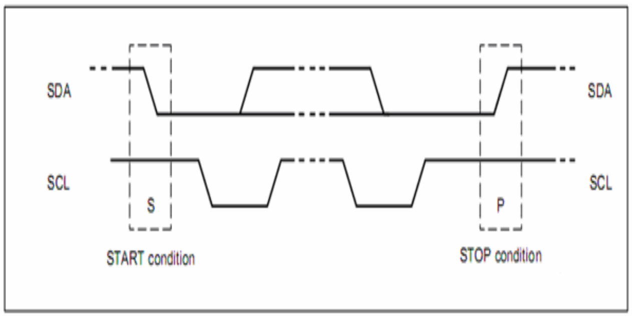
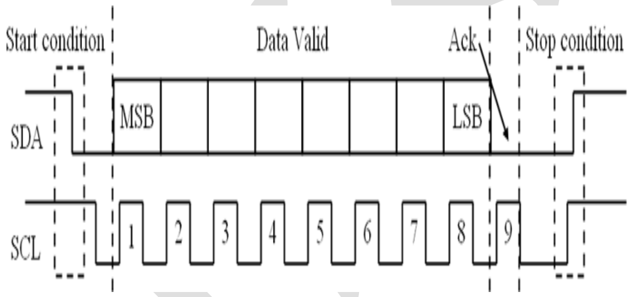


1.2 STARTING BYTES

The I2C bus is a byte-oriented protocol. After signaling Slaves by the Start condition, the Master sends “starting bytes” to the Slave. There are two components that make us the “starting bytes”: Slave address and data direction (Read or Write). The Master sends the MSB (Most Significant Bit) first and the LSB (Least Significant Bit) last. There are two addressing modes in the I2C protocol: the 7-bit and 10-bit address modes.

We will first consider the 7-bit addressing mode. After the STARTcondition (S), a Slave address is sent. This address is the first 7 bits, the eighthbit is a data direction bit (RnW). If the direction bit is ‘0’, it indicates atransmission (or WRITE). If the bit is ‘1’,it indicates a request for data (or READ).A data transfer is always terminated bya STOP condition (P) generated by the Master. However, a Master can generate a repeated START condition (Sr) and address another Slave without first generating a STOP condition.



When the I2C bus became more popular, it was recognized that the number of available addresses in the 7- bit addressing mode is too small.Therefore, a new addressing mode (the 10-bit mode) was developed. The new addressing mode also supports the old one. Devices with 7-bit addresses can beconnected with devices with 10-bit addresses on the same bus. In thismode, the first two bytes are dedicated for address and data direction. The format of the first byte is 11110xx; the last two bits of the first byte, combined with eight bits in the second byte form the 10-bit address.

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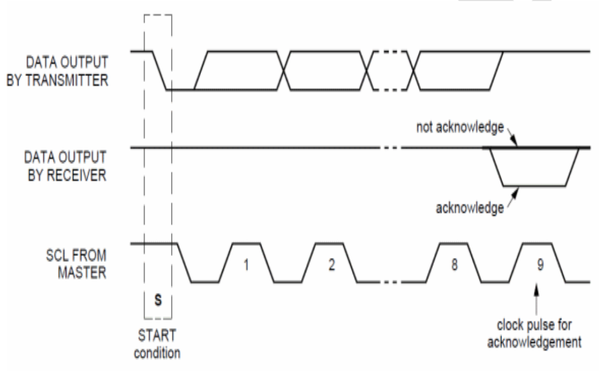
1.3 ACKNOWLEDGEMENT

Acknowledgement is obligatory in orderto inform the transmitter that data has been successfully transmitted. Figureillustrates the acknowledgement mechanism. The Master generates the acknowledgement related clock pulse and the transmitter releases the SDA line (HIGH) during the acknowledgeclock pulse so that the receiver can take control of the SDA line. If the receiver does not acknowledge, leaving the SDA line high, the transfer must be aborted.If it acknowledges by pulling the SDA line low, the transmitter knows that data has been successfully received, so itkeeps sending data to the receiver.



1.4 A COMPLETE DATA TRANSFER

All of the major aspects of I2C bus discussed so far are combined to create

complete data transfer from the transmitter to the receiver as in Figure 2.7. The SCL signal, Start and Stop signals, and the first byte must be generated by the Master. The Acknowledgement of the first byte must be generated by the Slave when it recognizes its address on the bus. The other Acknowledgements are generated by the receiver.

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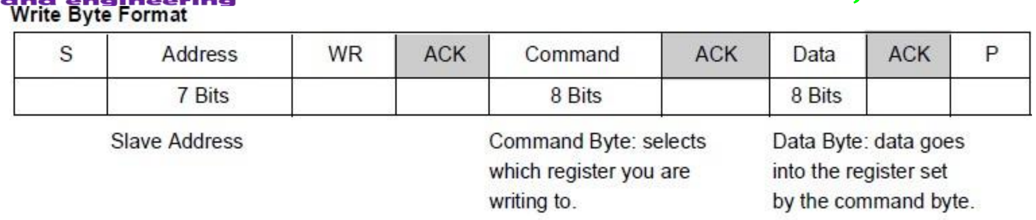


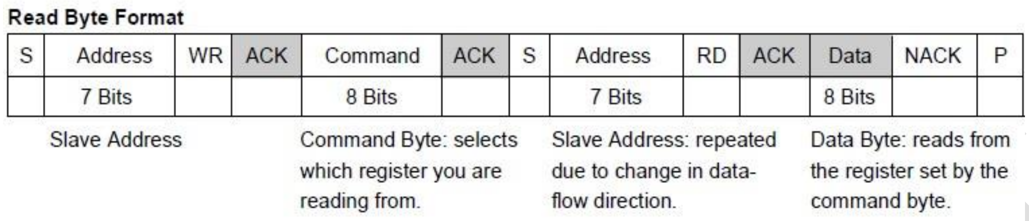
Write Byte Format

S	Address	WR	ACK	Command	ACK	Data	ACK	P
	7 Bits			8 Bits		8 Bits		

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.



Read Byte Format

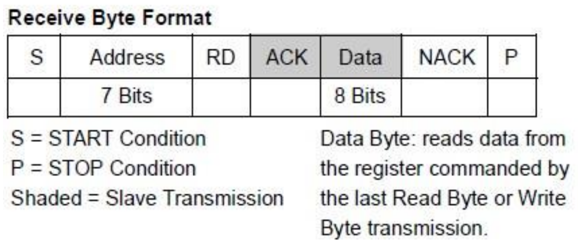
S	Address	WR	ACK	Command	ACK	S	Address	RD	ACK	Data	NACK	P
	7 Bits			8 Bits			7 Bits			8 Bits		

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data-flow direction.

Data Byte: reads from the register set by the command byte.



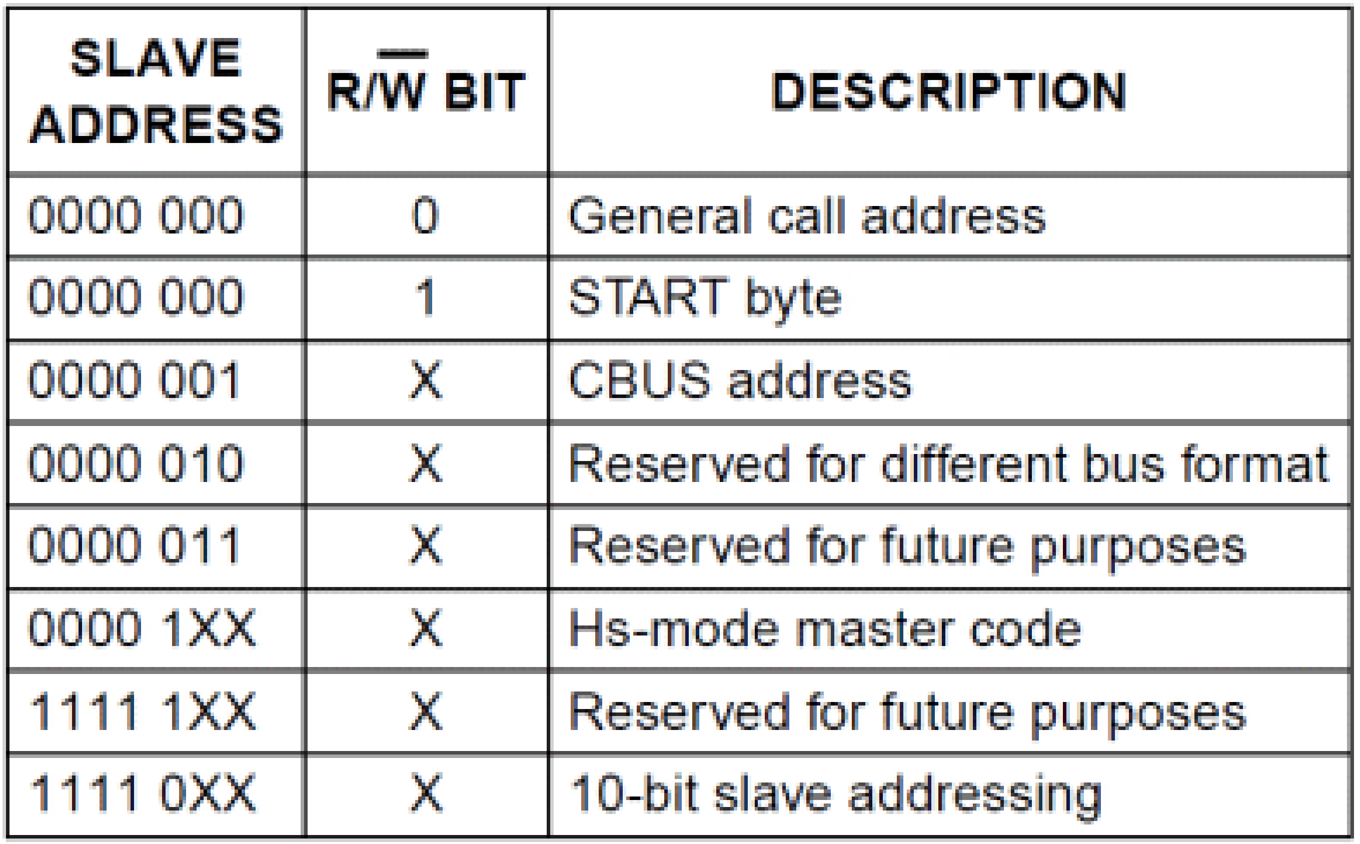
Receive Byte Format

S	Address	RD	ACK	Data	NACK	P
	7 Bits			8 Bits		

S = START Condition
P = STOP Condition
Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last Read Byte or Write Byte transmission.

1.5 7 BIT ADDRESS



SLAVE ADDRESS	$R/\overline{W}$ BIT	DESCRIPTION
0000 000	0	General call address
0000 000	1	START byte
0000 001	X	CBUS address
0000 010	X	Reserved for different bus format
0000 011	X	Reserved for future purposes
0000 1XX	X	Hs-mode master code
1111 1XX	X	Reserved for future purposes
1111 0XX	X	10-bit slave addressing

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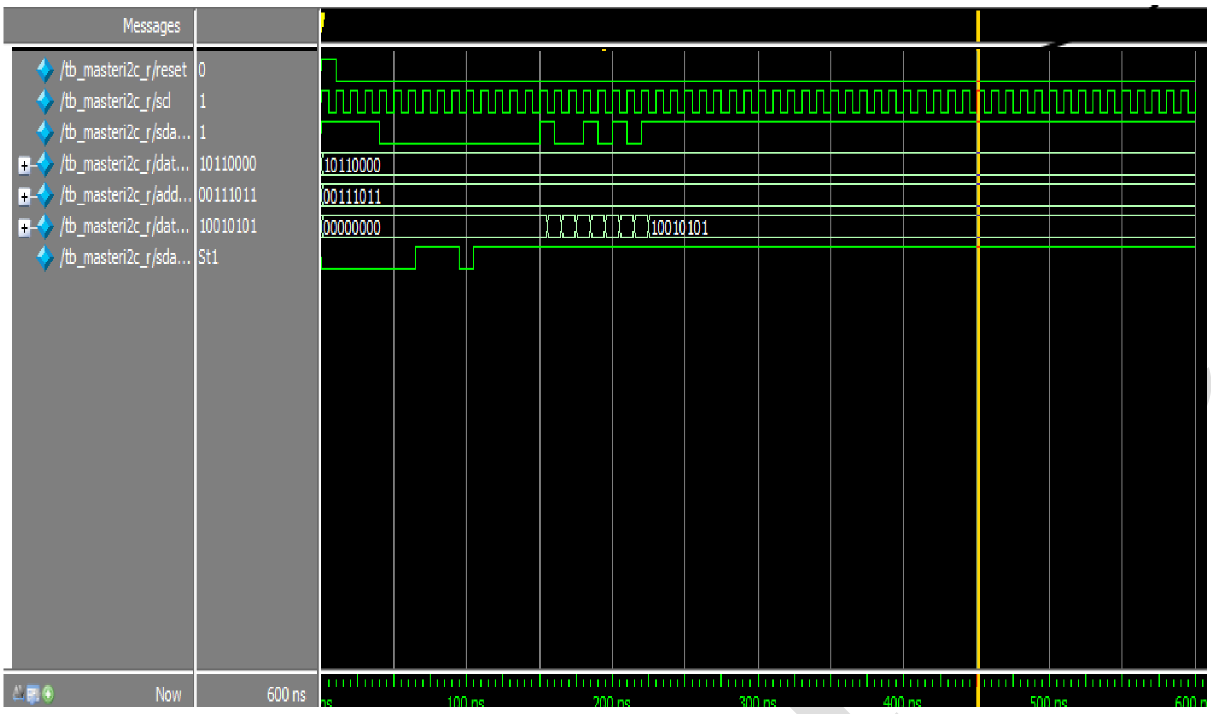
2. RESULTS



```
Messages
/tb_masteri2c_r/reset   0
/tb_masteri2c_r/scl     1
/tb_masteri2c_r/sda...  1
/tb_masteri2c_r/dat...  10110000    10110000
/tb_masteri2c_r/add...  00111011    00111011
/tb_masteri2c_r/dat...  10010101    00000000  10010101
/tb_masteri2c_r/sda...  St1
Now                     600 ns
```

2.1 SIMULATION AND TIMING DIAGRAM FOR READ OPERATION

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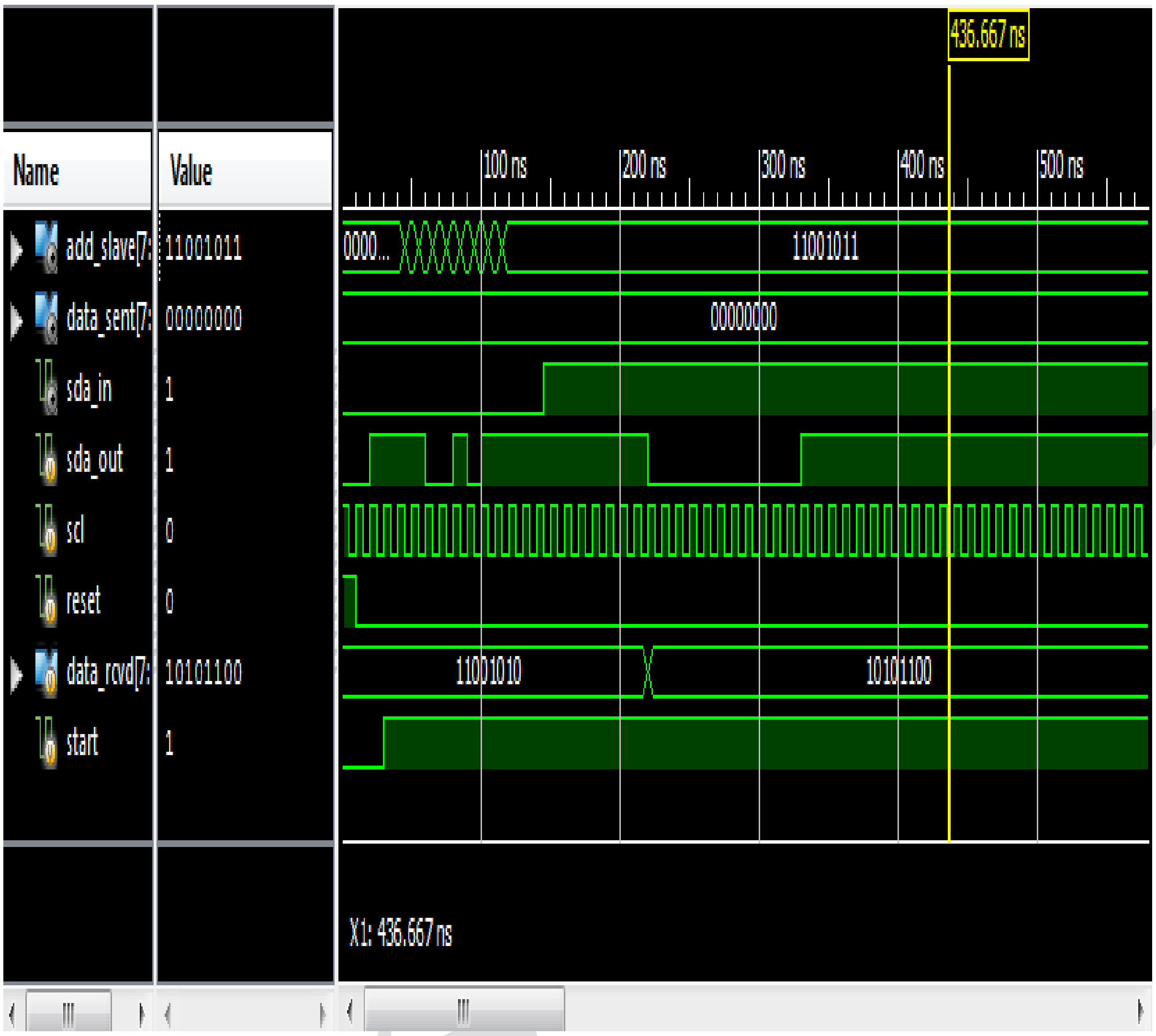
SIMULATION AND TIMING DIAGRAM FOR WRITE OPERATION



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3. CONCLUSION

In this paper designing of inter integrated circuit (I2C) using verilog in Modelsim- Altera 6.4a (Quartus 2nd edition 9.0) we have designed an interintegrated circuit (I2C). The I2C Bus is a two-wire, bi-directional serial bus that provides a simple and efficient method of data transmission over a short distance between many devices. Simulation is done with the help of coding in Modelsim- Altera 6.4aedition.

REFERENCE

1. ST24C02,ST Micro Electronics user manual.
2. I2C-Bus Specification, January 2000, Version 2.1.
3. Leens, Frederick. IEEE Instrumentation & Measurement Magazine, "An Introduction to I2C and SPI Protocols," February 2009.
4. Philips Semiconductors, "I2C Manual," Application Note, ref. AN10216-0, March 24, 2003, J. M. Irazabel & S. Blozis.M.B. Srinivas and Abinesh R. Bharghava. Low Power Data Coding Scheme for Synchronous Serial Communication based on Transition Inversion, IEEE Computer Society Annual Symposium on VLSI, 2009.
5. "Implementation of I2C Using System Verilog And FPGA," by S. Sobhan, S. Das, and I. Rahman, International Conference on Advancement in Electronics and Power Engineering, Bangkok, December 2011.
6. "FPGA Based Design & Implementation of Serial Data Transmission Controller" by Breakling A. Khan and A. Thakare, International Journal of Engineering Science and Technology 2010, pp. 5526–5533.